Analog-to-Digital Converter
Case Study

An 8-b 100-MSample/s CMOS Pipelined Folding ADC

• The concept of the two-stage and folding ADC:
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- Flash ADC:

- Folding ADC:
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- Folding amplifier:

![Folding Amplifier Diagram]

- Conventional folding ADC:

![Conventional Folding ADC Diagram]
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

• Folder design: \( k=4 \) and \( k=3 \)

• Pipeline folding ADC

Timing
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

• Top level block diagram

An 8-b 100-MSample/s CMOS Pipelined Folding ADC

• Second stage folder
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- INL due to gain mismatch

\[ Y_1 = G(1 + \alpha)x \]
\[ Y_2 = G(x - T) \]

Amplifier output

Interpolated signal

An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- Effect of tail current source mismatch

Tai-Cheng Lee
Spring 2011
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- comparator design

An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- conventional digital error correction
An 8-b 100-MSample/s CMOS Pipelined Folding ADC

- generic digital error correction

\[ D_{\text{OUT}} = N \times C_0 + C_1 \]

ADC coding (without error correction)

\[
\begin{array}{ccccccc}
0 & 1 & 2 & 3 & 0 & 1 & 2 \\
\text{Coarse ADC Code } C_0 & 0 & N-1 & 0 & N-1 & 0 & N-1 \\
\text{Coarse ADC Code } C_1 & 0 & N-1 & N & 2N-X & 2N & 3N-1 & 3N & 4N-1 \\
\end{array}
\]

(a)

ADC coding (with digital error correction)

\[
\begin{array}{ccccccc}
0 & 1 & 2 & 3 & 4 & 5 & 6 \\
\text{Coarse ADC Code } C_0 & 0 & N-1 & 0 & N-1 & 0 & N-1 \\
\text{Coarse ADC Code } C_1 & 0 & N-1 & 0 & N-1 & 0 & N-1 \\
\end{array}
\]

(b)

Digitally Calibrated Pipeline ADC

1. A 15-b 1-Msample/s digitally self-calibrated pipeline ADC

*Karanicolas, A.N.; Hae-Seung Lee; Barcrania, K.L.*

Page(s): 1207-1215, JSSC 1993 Dec
Digitally Calibrated Pipeline ADC -- I

• Ideal pipeline ADC:

![Diagram of Ideal Pipeline ADC]

Fig. 1. Pipeline ADC architecture

• Transfer characteristics:

![Diagram of Transfer Characteristics]

Digitally Calibrated Pipeline ADC -- I

• nonideality of transfer curve:

![Diagram of Nonideality of Transfer Curve]

Gain is less than 2 per stage
Digitally Calibrated Pipeline ADC -- I

- Top level diagram of “backward” calibration:

- Residue plot for gain <2 with comparator offset

Digitally Calibrated Pipeline ADC -- I

- Actual implementation of non-radix-2 ADC:
Pipeline ADC Design

- T. Cho's thesis (UC Berkeley)

kT/C noise (I)

- RMS voltage for kT/C noise:

<table>
<thead>
<tr>
<th>C</th>
<th>$\sigma = \sqrt{kT/C}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01pF</td>
<td>640μV</td>
</tr>
<tr>
<td>1pF</td>
<td>64μV</td>
</tr>
<tr>
<td>100pF</td>
<td>6.4μV</td>
</tr>
</tbody>
</table>

TABLE 2. RMS values for the thermal noise for different sampling capacitor values at room temperature
kT/C noise (II)

- The bottom line for a switched-cap circuit for different capacitance

\[ \text{SNR(dB)} \]

\[ \begin{align*}
85.00 & \quad \text{14bit} \\
80.00 & \quad \text{12bit} \\
75.00 & \quad \text{10bit} \\
70.00 & \quad \text{8bit} \\
65.00 & \\
60.00 & \\
55.00 & \\
50.00 & \\
45.00 & \\
40.00 & \end{align*} \]

\[ \begin{align*}
\text{V}_{\text{in}} & \quad \rightarrow \quad \text{C}_{\text{F}} \quad \rightarrow \quad \text{V}_{\text{out}} \\
\text{V}_{\text{in}} & \quad \rightarrow \quad \text{C}_{\text{F}} \quad \rightarrow \quad \text{C}_{\text{S}} \\
\text{V}_{\text{in}} & \quad \rightarrow \quad \text{+2Q}_{\text{in}} \quad \rightarrow \quad \text{V}_{\text{out}} \\
\text{V}_{\text{in}} & \quad \rightarrow \quad \text{H}_{\text{F}} \quad \rightarrow \quad \text{V}_{\text{out}} \\
\text{V}_{\text{in}} & \quad \rightarrow \quad \text{+0} \quad \rightarrow \quad \text{V}_{\text{out}} \\
\end{align*} \]
Noise in OP amp (I)

- Single-stage op amp

Noise in OP amp (II)

- Two-stage op amp
OP amp based SHA (I)

- Different OP amp SHA

<table>
<thead>
<tr>
<th>Transfer Function (V_{out}/V_{in})</th>
<th>Feedback Factor (f)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{C_S}{C_F}$</td>
<td>$\frac{C_F}{C_S + C_F + C_{opamp}}$</td>
</tr>
<tr>
<td>$1$</td>
<td>$\frac{C_S}{C_S + C_{opamp}}$</td>
</tr>
<tr>
<td>$1 + \frac{C_S}{C_F}$</td>
<td>$\frac{C_F}{C_S + C_F + C_{opamp}}$</td>
</tr>
</tbody>
</table>

OP amp based SHA (II)

- How to pick the optimal sampling capacitor
OP amp based SHA (III)

- An optimal sampling capacitor can be obtained.

Normalized time constant ($\tau/\tau_i$) vs. $I_{ds}$
- $\rho = 1\,\mu A/\mu m$
- $L = 1.2\,\mu m$
- $k_p = 60\,\mu A/V^2$

Optimum-settling time constant when $I_{ds} = 1\,mA$

OP amp based SHA (V)

- Other design considerations:
  1. Gain error
  2. Slew rate

\[ V_{out} = \frac{C_S}{C_F} \cdot V_{in} \]

Does it matter?

(2) Slew rate

\[ V = SRxt \]
\[ V = V_f(1 - \exp(-t/\tau)) \]
OP amp based SHA (IV)

- Other design considerations:
  (3) switch on resistance:

![Diagram of OP amp based SHA (IV)](image)

High-Speed Pipelined ADC

- ADC top level diagram:

![Diagram of High-Speed Pipelined ADC](image)
High-Speed Pipelined ADC

- feedback factor and load capacitance for different resolution

<table>
<thead>
<tr>
<th>B</th>
<th>( f )</th>
<th>( C_{LT} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( \frac{C_i}{2 \cdot C_i + C_{\text{opamp}}} )</td>
<td>( \frac{C_i [2C_i + C_{\text{opamp}}]}{2C_i + C_{\text{opamp}}} + 2C_{i+1} + 2C_{\text{comp}} )</td>
</tr>
<tr>
<td>2</td>
<td>( \frac{C_i}{4 \cdot C_i + C_{\text{opamp}}} )</td>
<td>( \frac{C_i [4C_i + C_{\text{opamp}}]}{4C_i + C_{\text{opamp}}} + 4C_{i+1} + 6C_{\text{comp}} )</td>
</tr>
<tr>
<td>3</td>
<td>( \frac{C_i}{8 \cdot C_i + C_{\text{opamp}}} )</td>
<td>( \frac{C_i [8C_i + C_{\text{opamp}}]}{8C_i + C_{\text{opamp}}} + 8C_{i+1} + 14C_{\text{comp}} )</td>
</tr>
</tbody>
</table>

High-Speed Pipelined ADC

- digital correction

\[ V_{\text{out}} \]

\[ V_{\text{in}} \]

\[ V_{\text{in}} \rightarrow \text{Stage} \rightarrow V_{\text{out}} \]

B+1 bits

Offset Correction Range

\[ -\frac{5}{8} - \frac{3}{8} - \frac{1}{8} \]

\[ \frac{3}{8} \frac{5}{8} \]
High-Speed Pipelined ADC

- subtractor implementation: R-DAC and C-DAC

High-Speed Pipelined ADC

- The requirement of stage accuracy
High-Speed Pipelined ADC

- The requirement of stage accuracy

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Minimum requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op amp DC gain</td>
<td>( \Delta &gt; (2^{N-1})/f &gt; 2^N )</td>
</tr>
<tr>
<td>Settling time</td>
<td>( \tau &lt; 1/(2 \text{ fs } N \ln(2.0)) )</td>
</tr>
<tr>
<td>(assuming single pole response)</td>
<td></td>
</tr>
<tr>
<td>DAC accuracy</td>
<td>(</td>
</tr>
<tr>
<td>Noise</td>
<td>( \sigma_{\text{total, i}} &lt;&lt; \text{ LSB}(=V_{\text{FS}}/2^N) )</td>
</tr>
</tbody>
</table>

High-Speed Pipelined ADC

- The power dissipation vs. sampling frequency for various resolution ADCs:

![Graph showing power dissipation vs. sampling frequency](image)
High-Speed Pipelined ADC

- Different resolutions for each stage:

- Scaling for each stage:
High-Speed Pipelined ADC

- Total power for scaling and non-scaling ADC:

Low-Power Low-Voltage Pipelined ADC

- 1.5 bits per stage:
Low-Power Low-Voltage Pipelined ADC

- Digital error correction:

- First-stage SHA:
Low-Power Low-Voltage Pipelined ADC

• Timing for pipeline ADC

![Timing diagram for pipeline ADC](image)

Dynamic Comparator

• A dynamic comparator with built-in threshold generator:

![Dynamic Comparator diagram](image)
Low-voltage OP

• A 3.3-Volt OP amp

Low-voltage OP

• Output CMFB circuit
Low Voltage Operation of SC Circuits

• CMOS switch

\[ G_{on} = g_{dsn} + g_{dsp} \]

- Conductance vs. Voltage
  \( V_{thn} = |V_{thp}| = 0.8V \)
  - GND
  - \(-V_{thp}\)
  - \(-V_{thn}\)
  - GND
  - Vdd = 3.3V
  - GND
  - Vdd = 1.5V

Low Voltage Operation of SC Circuits

• Boosted circuit:

\[ V_{dd} = 3.3 \text{ V} \]

\[ V_{sub\_hi} \]

\[ V_{hi} = \sim 5 \text{ V} \]

\[ 0 \]

\[ 3.3 \text{ V} \]

NMOS only!
Low Voltage Operation of SC Circuits

- Floating well to prevent latch up:

A 0.02-mm² 9-bit 50-MS/s Cyclic ADC in 90-nm Digital CMOS
Conventional Cyclic ADC

\[ V_O = 2V_{in} + DV_{REF} \]

- \((N+1)\) clock cycles to do the \(N\)-bit conversion.
- Minimum area among all types of ADCs.


Prior Arts (I)

- Opamp shared between phases.
  - Only one opamp required.
  - Two phases for one-bit conversion.

\( JSSC 99' \), S. H. Lewis, et al
Prior Arts (II)

- Opamp shared between phases.
  - Only one opamp required.
  - Two phases for one-bit conversion.
  - Different feedback factors.

Prior Arts (III)

- Two residue gain stages.
  - One phase for one-bit conversion.
  - Two opamps.
Multiply-by-Two Gain Stage

\[ V_{in} \times C + D V_{ref} \times \frac{C}{2} = V_{res} \times C - V_{res} \times \frac{C}{2} \]
\[ V_{res} = 2V_{in} + D V_{ref} \]

- Partial positive-feedback loop
  - The amplification, subtraction of sub-DAC are performed in charge domain.

Proposed 9-bit Cyclic ADC

- Feedback C stores the residues.
- Four clock cycles to perform the conversion.
Small-Signal Analysis

\[ V_{out} = \frac{g_{m1}g_{m2}g_{m3}}{s^3 + s^2 (\frac{3g_{m2}C_C - g_{m1}C_C + 8g_{m2}C}{8C(C_C + C_i)}) + s^2 (\frac{3g_{m2}g_{m3}C_C}{8C \cdot C_2 (C_C + C_i)}) + \frac{g_{m1}g_{m2}g_{m3}}{8C \cdot C_2 (C_C + C_i)}}] \]

\[ D(s) = s^3 + s^2 \left( \frac{g_{m1}}{4C(1 + \alpha_1)} \right) + s \frac{3g_{m2}g_{m3}C_C}{8C \cdot C_2 (1 + \alpha_1)} + \frac{g_{m1}g_{m2}g_{m3}}{8C^2 \cdot C_2 \gamma_1 (1 + \alpha_1)} \]

\[ = (s + \omega_{c1})(s^2 + 2\zeta\omega_{n}s + \omega_n^2) \]

S-Plane Pole Position

\[ D(s) = (s + \omega_c)(s^2 + 2\zeta\omega_n s + \omega_n^2) \]

err: \( e^{-\omega_c t} \)

\[ err: e^{-\zeta\omega_n t} \left[ \cos(\omega_n \sqrt{1-\zeta^2} t) + \frac{\zeta\omega_n}{\omega_n \sqrt{1-\zeta^2}} \sin(\omega_n \sqrt{1-\zeta^2} t) \right] \]

- Pole location characterizes closed-loop step response.
Small Signal Analysis (cont’d)

- Faster linear settling is achieved if both circuits are designed to have the same settling behavior.

\[
\omega_C = \frac{2\zeta_1 \omega_{n1}}{2\zeta_2 \omega_{n2}} = \frac{g_m}{4C(1+\alpha_1)} \left( \frac{1 + \frac{5}{\gamma_2}}{1 + \frac{4}{\gamma_1}} \right)
\]

Current-Steering T/H

- Fast-switching between track and hold phases.
**Transient Response of the T/H**

\[ t_d \approx 0.1 \text{ns}, \; f = 100 \text{ MHz}, \; C = 500 \text{ fF}, \; R \approx 100\Omega \]

\[ V = V_1 + V_2 = (\omega t_d)A \cos \omega t + (\omega RC)A \cos \omega t \approx 0.094A \cos \omega t \]

Less than 10% of the full swing range

- The transient depends on:
  - Small delay for the bottom plate sampling.
  - Finite switch ON resistance.

**Timing for the ADC**

- The short hold time \( t_H \) occupies only a small fraction of the conversion time.
Track-and-Evaluation Characteristic

- Output is equivalent to be precharged to the input voltage before evaluation.

Circuit Schematics - Opamp

- Two-stage architecture.
- Output stage for T/H function.
- 5.3 mW with a 1-V power supply.
- Preamplifier reduces the equivalent offset.
- Power of the preamplifier $\sim 0.1$ mW.

- Provide the reference voltages on chip.
- Consume 4 mW in this work.
90-nm Digital CMOS
  - With pads: 860 µm × 860 µm
  - Active area: 194 µm × 96 µm = 0.0186 mm²

Experimental Results @ 50 MS/s

\[ f_{in} = 1\text{MHz} @ f_s = 50\text{MHz} \]
- SNDR = 50.5 dB
- SFDR = 66.8 dB

\[ f_{in} = 20\text{MHz} @ f_s = 50\text{MHz} \]
- SNDR = 50.2 dB
- SFDR = 61.4 dB
Experimental Results - DNL / INL

- DNL : 0.43/-0.47 LSB
- INL : 0.63/-0.60 LSB

Dynamic Performance Summary

- SNDR v.s. Sampling Freq. (f_{in} = 1 MHz)
- SNDR v.s. Input Freq. (f_s = 50 MHz)
A 10-bit 100-MS/s Pipelined ADC with a Time-Sharing Technique
Pipelined Stage

- Sub-ADC errors are corrected by DEC.
- DAC & gain stage still require full accuracy.
  → High-gain, wide-bandwidth opamp is essential.

Conventional 10-b Pipelined ADC

- Lower resolutions at backend stages.
- Opamps consume most power.
Prior Arts (I) – Zero-Cross Based Detector

- Replace opamp with a zero-crossing detector.
  - Almost no static current consumption.
  - Open-loop operations.

Prior Arts (II) – Dynamic SF Amplification

- Dynamic source follower amplification
  - No static currents.
  - Inaccurate conversion gain.

\[
G \approx - \frac{C_{gs} + C_{gd} + C_{gb}}{C'_{gd}}
\]

JSSC 09’, L. Brook, et al

JSSC 09’, J. Hu, et al
Prior Arts (III) – Capacitive Charge Pump

- Passive multiply-by-two
  - High-gain opamp is not required.
  - Open-loop operations.
  - Inaccurate conversion gain caused by parasitics.
  - Driving buffer still consumes static power.

Prior Arts (IV) - Opamp Sharing

- Reduce the number of required opamps.
  - Compact architecture.
  - Opamp power is limited by MDAC j.
Different Evaluation Time

- Only reserve half of $T_S$ for MDAC (j+1).
- Opamp is turned off during the rest of $T_S$.
  $\rightarrow$ Equivalent power consumption is halved.

Evaluation Time Sharing

- Opamp is reused by the next stage.
- Opamp shared between three MDAC stages.
Proposed Architecture

- One opamp to complete 10-b conversion.

Capacitance Scaling

\[ \frac{T_{S1}}{T_{S2}} = \frac{n_1 C_{L1,tot}}{n_2 C_{L2,tot}} = \frac{9 \times 1.75C}{7 \times 0.9875C} \approx 2.3 \]

- Capacitance is scaled to apply the time sharing technique.
Input Sampling Network

- Delay mismatch should be less than 0.2 ns within the Nyquist band.
- RC time constants are designed equal.

\[
\Delta V \approx \frac{dV_{in}}{dt} \times t_d \leq A\omega_{in} \times t_d = \frac{V_{REF}}{16}
\]

\[
R_{on,A/ID} \times C_{A/ID} = R_{on,MDAC} \times C_{MDAC}
\]

Opamp Design (I)

- Based on the 1\(^{st}\)-order settling assumption.
  - Opamp is limited to one-stage architecture.
  - Difficult to achieve a high-gain and wide-swing design.
Opamp Design (II)

\[ \beta g_m > \frac{C_C}{T_S} \times n \times \ln 2 \]

\[ \text{PM} \approx 90^\circ - \tan^{-1} \frac{\omega'_t}{\omega'_p} = 90^\circ - \tan^{-1} \frac{\omega_t}{\omega_p} \]

\[ \frac{\omega_t}{\omega'_p} = \frac{\omega_t}{\omega_p} \approx \frac{g_{m1}/C_C}{g_{m2}/C_{L,tot}} \propto \frac{C_{L,tot}}{C_C} \]

- \( C_C \) is adjusted for different loop BW.

Opamp Design (III)

- Two-stage architecture.
- Power consumption : 3.0 mW (including bias circuit).
Opamp Design (IV)

- Dual input pairs for removing the parasitic charge.
  → Avoid sample-to-sample memory effects.

MDAC Stages

- Loading capacitance reduces the loop BW.
Capacitor Sharing Technique (I)

- Settling accuracy is improved.

\[(JSSC 09', N. Sasidhar; JSSC 09', B.-G. Lee; JSSC 07', P. Y. Wu.)\]

\[C_{L1,\text{tot}} : 1.75C \rightarrow 0.75C\]

Capacitor Sharing Technique (II)

- Loading of 2nd stage is identical to 1st stage.
  \[\Rightarrow C_C \text{ needs not to be switched to obtain the best phase margin.}\]
Capacitor Sharing Technique (III)

Charge stored on node $V_{in}$:

$$V_{res1} = \frac{V_{res1}}{A} C_1 + \frac{V_{res1}}{A} C_p + (\frac{V_{res1}}{A} + \frac{V_{res2}}{A})(C_{21} + C_{22})$$

Do not affect $V_{res2}$

$$V_{res2} = \frac{V_{res1}}{\beta} \left(1 - \frac{1 + \beta C_p/C_{22}}{A} \left(1 - \frac{1}{\beta}\right)\right) \approx \frac{V_{res1}}{\beta} \left(1 - \frac{1}{\beta \cdot \frac{4A}{3}}\right)$$

- Effective gain is increased by 2.5 dB.

Power Comparison

<table>
<thead>
<tr>
<th></th>
<th>1st Stage</th>
<th>2nd Stage</th>
<th>3rd Stage</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Scaling</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>Stage Scaling</td>
<td>1</td>
<td>$R_1$</td>
<td>$R_1R_2$</td>
<td>$1+R_1+R_1R_2$</td>
</tr>
<tr>
<td>Opamp Sharing</td>
<td>0.5</td>
<td>0.5</td>
<td>$R_1R_2$</td>
<td>$1+R_1R_2$</td>
</tr>
<tr>
<td>Time Sharing</td>
<td>0.5</td>
<td>0.25</td>
<td>0.25</td>
<td>1</td>
</tr>
<tr>
<td>Cap. Sharing &amp; Optimal Timing</td>
<td>0.33</td>
<td>0.25</td>
<td>0.25</td>
<td>0.83</td>
</tr>
</tbody>
</table>

- $R_1$ equals to 0.25 theoretically.
  - Considering to the slew rate, $R_1$ usually is larger than 0.25.
90-nm Digital CMOS
- With pads: 860 \( \mu \text{m} \times 860 \mu \text{m} 
- Active area: 220 \( \mu \text{m} \times 260 \mu \text{m} = 0.0572 \text{mm}^2

Measured Spectrums @ 100MS/s

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>SNDR (dB)</th>
<th>SFDR (dB)</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>55.0</td>
<td>62.3</td>
<td>56.3</td>
</tr>
<tr>
<td>50 MHz</td>
<td>53.9</td>
<td>67.4</td>
<td>54.4</td>
</tr>
</tbody>
</table>
DNL/INL @ 100MS/s, 10-b

- DNL : 0.81/-0.62 LSB
- INL : 1.00/-0.89 LSB

Dynamic Performance Summary
### Performance Summary Table

<table>
<thead>
<tr>
<th>Technology</th>
<th>90-nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10 bit</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Signal Swing</td>
<td>600 mV&lt;sub&gt;dpp&lt;/sub&gt;</td>
</tr>
<tr>
<td>SNDR @ f&lt;sub&gt;in&lt;/sub&gt; = 10 MHz</td>
<td>55.0 dB</td>
</tr>
<tr>
<td></td>
<td>@ f&lt;sub&gt;in&lt;/sub&gt; = 20 MHz</td>
</tr>
<tr>
<td></td>
<td>@ f&lt;sub&gt;in&lt;/sub&gt; = 50 MHz</td>
</tr>
<tr>
<td></td>
<td>@ f&lt;sub&gt;in&lt;/sub&gt; = 99 MHz</td>
</tr>
<tr>
<td>DNL</td>
<td>0.81/-0.62 LSB</td>
</tr>
<tr>
<td>INL</td>
<td>1.00/-0.89 LSB</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>10.7 mW</td>
</tr>
<tr>
<td></td>
<td>- Core Converter</td>
</tr>
<tr>
<td></td>
<td>- Reference Buffer</td>
</tr>
<tr>
<td>Die Area</td>
<td>0.74 mm&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>- Active(w/o buffers)</td>
</tr>
</tbody>
</table>

- **Power Consumption**
  - Analog: 3.7mW
  - Digital: 0.8mW

FoM = \( \frac{\text{power}}{2^{\text{ENOB}} \times \text{sampling rate}} \)

\[ \text{FoM} = 98 \text{ fJ/Conv.} = 233 \text{ fJ/Conv.} \]

(including ref. buffer)